REMARKS

In reference to Fig. 1(A), claim 3 has been amended to recite that the printed wiring substrate comprises a dielectric layer 28 covering the front surface 3 of the core substrate 2; terminal electrodes 32 (solder bumps) for mounting a semiconductor element 34 (IC chip) on the front surface of the printed wiring substrate; and via conductors 24 penetrating the dielectric layer 28 and connecting at least one of the terminal electrodes 32 to the electrode 12 of the electronic component 10 (chip capacitor). This is described at pages 13-18 of the specification.

Claim 3 has also been amended to provide antecedent basis with respect to the height of the electrode as claimed in claims 4 and 6.

Claim 3 is generic to both claims 13 and 14. Claims 5 and 8 depend from claim 14. If generic claim 3 is allowable, then so is non-elected claim 14 and claims 5 and 8 depending from claim 14.

Non-elected method claims 11 and 12 have been amended to specifically include all of the limitations of claims 13 and 14, respectively. Applicants respectfully request rejoinder of method claims 11 and/or 12 under MPEP § 821.04 if claims 13 and/or 14 are found to be patentable.

Entry of the amendments and review and reconsideration on the merits are requested.

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,338,767 to Nakatani et al in view of U.S. Patent 5,776,551 to Pasch and U.S. Patent 5,335,139 to Nomura et al.

Nakatani et al Fig. 4 was cited as disclosing a printed wiring substrate including embedded electronic component 403, where the core substrate contains an inorganic filler having an average particle size of 0.01 μm to 10 μm (col. 11, lines 7-35, actually 0.1 μm to 100 μm). Although acknowledging that Nakatani et al fails to explicitly disclose an electrode projecting from an upper or lower end of the electronic component, the Examiner further cites to col. 9, lines 15-24 and Fig. 2 as disclosing that projecting electrodes in the form of solder bumps 205 may be formed on circuit component 204, subsequently embedded in resin sheet 200.

Pasch was cited as disclosing a flip chip die having bump electrodes.

Nomura et al was cited as disclosing a chip capacitor having external electrodes 4 ranging in thickness from about 10 to 50 μm (col. 6, lines 53-59).

The reason for rejection was that it would have been obvious to modify the electronic component of the board of Nakatani et al to have a projecting electrode, as taught by Pasch and Nomura, and as further suggested by Nakatani et al (solder bumps 205 and Fig. 2) so as to provide reliable electric connection and so as to maintain a desired gap between the component body and the connecting electrode/pad of the substrate.

Applicants respectfully traverse for the following reasons.

As required by amended claim 3, in addition to an electrode projecting from at least an upper end of the electronic component, the printed wiring substrate further comprises a dielectric (i.e., insulating) layer covering the front surface of the core substrate, terminal electrodes for mounting a semiconductor element on the front surface of the printed wiring substrate, and via conductors penetrating the dielectric layer and connecting at least one of the terminal electrodes

to the electrode of the electronic component. Therefore, *assuming arguendo* that Fig. 2 of Nakatani et al discloses projecting electrodes in the form of solder bumps 205 formed on circuit component 204, and subsequently embedded in resin sheet 200, the resulting structure lacks via conductors penetrating a dielectric layer covering the front surface of the core substrate and connecting a terminal electrode for mounting a semiconductor element on the surface of the printed wiring substrate to an electrode of the electronic component.

Pasch (flip chip die having bump electrodes) and Nomura et al (chip capacitor) also fail to disclose the above-noted limitations of amended claim 3.

For the above reasons, it is respectfully submitted that claim 3 is patentable over Nakatani et al in view of Pasch and Nomura et al.

Applicants further comment on the cited prior art as follows.

Die 102 of Pasch has solder bumps 104 for flip-chip attachment, for example, to a circuit board (Abstract). There is nothing in Pasch which relates to embedding the die in a printed wiring substrate or otherwise. Similarly, the multilayer ceramic chip capacitor of Nomura et al is mounted on a printed circuit board (col. 9, lines 24-27). Thus, there is nothing in the cited prior art which would teach the desirability of employing the die of Pasch having solder bumps for the chip capacitor of Nomura et al having external leads as an embedded circuit component in the circuit board of Nakatani et al. In fact, similar to Pasch and Nomura et al, Fig. 4 of Nakatani et al mainly relied upon by the Examiner is also directed to flip chip bonding of the component 403 (col. 11, lines 52-56), which is an additional reason as to why the prior art does not suggest the desirability of providing the electronic component with electrodes projecting from an upper end

thereof (and connected to terminal electrodes for mounting a semiconductor element by means of via conductors penetrating a dielectric layer).

Withdrawal of the foregoing rejection under 35 U.S.C. § 103(a) is respectfully requested.

Claims 6 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Nakatani et al, Pasch and Nomura et al, further in view of U.S. Patent 6,129,955 to Papathomas et al.

As noted by the Examiner, Nakatani et al contemplates the use of an inorganic filler to allow for improved heat dissipation (col. 2, lines 49-63), and contends that in order to improve the heat dissipation rate, one of ordinary skill would have been led to employ a filler size much smaller than the gap between the component and the contact pad of the connecting substrate (i.e., the height of the projecting electrode). Papathomas et al was cited as disclosing encapsulating with a resin containing a thermally conductive filler, and having a particle size of from 0.5 μm to about 31 μm to allow the uncured composition to readily flow between the housing 31 and the substrate 11 (col. 14, line 65 to col. 15, line 23).

The reason for rejection was that it would have been obvious to employ, in the board of Nakatani et al, an inorganic filler having a particle size of not greater than 25 μm and half the height of the electrode as taught by Papathomas et al in order to improve heat dissipation rate.

Applicants respectfully traverse for the following reasons.

Like Pasch and Nomura et al, Papathomas et al (electronic package encapsulating a solder joint with an epoxy resin) likewise does not cure the deficiencies of Nakatani et al. Particularly, Papathomas et al does not disclose a dielectric layer covering the front surface of

the core substrate, terminal electrodes for mounting a semiconductor element on the front surface of the printed wiring substrate, and via conductors penetrating the dielectric layer and connecting at least one of the terminal electrodes to the electrode of the electronic component. Therefore, as above, it is respectfully submitted that a *prima facie* case of obviousness has not been established with respect to the amended claims. All claim limitations must be taught or suggested by the combined references in order to support an obviousness rejection - MPEP §2143.03.

For the above reasons, it is respectfully submitted that claims 6 and 9 are patentable over the combination of Nakatani et al, Pasch and Nomura, further in view of Papathomas et al.

Applicants further comment on the cited prior art as follows.

Papathomas et al relates to encapsulating a solder joint 53 between lead 51 and conductor 17 with epoxy resin (encapsulant) 61 containing silica filler (Abstract, Fig. 3 and col. 7, lines 63-67). The filler has a particle size of 31 μm or less, so that the uncured material can readily flow before polymerization (col. 15, lines 14-21).

Papathomas et al has nothing to do with particle size of the filler relative to height of a projecting lead. Furthermore, the encapsulation in Papathomas et al is external to an electronic component, and has nothing to do with embedding an electronic component in a printed wiring substrate.

In the present invention, an inorganic filler having a particle size of not greater than 25 μm and an electrode having a height of not lower than 50 μm is employed so as to appropriately reinforce a thin resin portion of the core substrate adjacent to the upper or lower end of an

electronic component from which an electrode projects, to prevent cracking or separation (page 7, lines 17-21 of the specification).

On the other hand, the Examiner considered that a filler size smaller than the gap between the component and the contact surface of the connecting substrate would be inherent in Nakatani et al so as to allow the filler to be present around the electrode and the component and thereby improve heat dissipation rate. However, such disclosure is nowhere to be found in Nakatani et al. Moreover, one of ordinary skill could not have arrived at the present invention in the absence of Applicants' teachings. See, for example, page 5, lines 3-5 of the specification which informs that the silica filler has a small particle size so as to readily enter even a thin resin portion extending between the upper or lower end of the chip capacitor 10 and the surface of the resin 13.

Withdrawal of the foregoing rejection under 35 U.S.C. § 103(a) is respectfully requested.

Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,324,067 to Nishiyama in view of Nakatani et al. Nishiyama's Fig. 6 was cited as disclosing an electronic component 4 embedded in a core substrate via sealing resin 9, the electronic component 4 having an electrode projecting from at least either an upper or lower end thereof. The reason for rejection was that it would have been obvious to incorporate an inorganic filler of Nakatani et al in the sealing resin of Nishiyama in order to improve heat dissipation.

Claims 4, 7 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Nishiyama and Nakatani et al, further in view of Pasch, Nomura et al and Papathomas et al. The reason for rejection was that it would have been obvious to provide a

filler having a particle size as small as possible as compared to the height of the electrode of the electronic component in order to enhance heat conduction rate.

Applicants respectfully traverse for the following reasons.

Applicants rely on the response above with respect to the rejection of claim 3 over Nakatani et al in view of Pasch, Nomura et al and Papathomas et al. Nishiyama adds nothing which would adversely affect patentability of amended claim 3 or claims 13 and 4, 7 and 10 which depend primarily or secondarily from claim 3.

Fig. 6 in Nishiyama cited by the Examiner does not show the above-noted features of amended claim 3. In Fig. 10, adhesive resin 14 does not embed component 4.

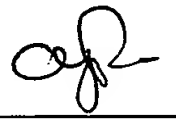
For the above reasons, it is respectfully submitted that claims 13, 4, 7 and 10 are patentable over the cited references, and withdrawal of the foregoing rejections under 35 U.S.C. §103(a) is respectfully requested.

Withdrawal of all rejections and allowance of claims 3-14 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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